What is claimed is:

1. A double corner rounding process for a partial vertical cell, comprising:

providing a substrate comprising a memory cell array region and a supporting region and having a first mask layer thereon, wherein a deep trench is formed in the first mask layer and the substrate in the memory cell region, a capacitor is formed in a lower portion of the deep trench, a first insulating is formed in the upper portion of the deep trench, and the surface of the first insulating layer is lower than that of the substrate;

filling a second mask layer in the deep trench, wherein the surface of the second mask layer is lower than that of the first mask layer;

forming a photoresist layer on the active areas of the substrate, such that a first portion of the substrate, covered by the photoresist layer, and a second portion of the substrate, not covered by the photoresist layer, are defined;

removing parts of the first mask layer not covered by the photoresist layer and the second portion of the substrate until the surface of the second portion of the substrate is lower than that of the first mask layer;

removing the photoresist layer and the second mask layer;

removing the edge of the first mask layer until the corner of the first portion of the substrate is exposed;

performing a first rounding process on the corner of the first portion of the substrate;

conformally forming a second insulating layer on the first mask layer , the first insulating layer, and the substrate;

forming an insulating plug on the second insulating layer, such that the surface of the insulating plug is substantially level with that of the second insulating layer on the substrate;

removing the insulating plug, the second insulating layer, and the first mask layer from the memory cell array to expose the corner of the first portion of the substrate;

performing a second rounding process on the corner of the substrate in the memory cell array region.

2. The method as claimed in claim 1, wherein the first mask layer comprises stacked silicon oxide and silicon nitride layers.

3. The method as claimed in claim 1, wherein the second mask layer is an organic anti-reflection coating layer.

4. The method as claimed in claim 3, wherein removal of the edge of the first mask layer is performed by anisotropic etching.

5. The method as claimed in claim 4, wherein an etching solution comprising hydrogen fluoride (HF) and ethylene glycol (EG) is employed in anisotropic etching.

6. The method as claimed in claim 1, wherein the first rounding process comprises oxidizing the corner and the sidewall of the first portion of the substrate to form a sacrificial oxide layer and removing the sacrificed oxide layer.

7. The method as claimed in claim 6, wherein oxidization is performed by in-situ steam generation (ISSG).

8. The method as claimed in claim 1, wherein the second insulating layer comprises silicon nitride.

9. The method as claimed in claim 1, wherein the insulating plug comprises silicon oxide formed by high density plasma chemical vapor deposition (HDP CVD).

10. The method as claimed in claim 8, wherein the second rounding process is performed by employing an oxidation agent and a HF solution by turns.

11. The method as claimed in claim 10, wherein the oxidation agent comprises $H_2O_{2(aq)}$ and $HNO_{3(aq)}$.

12. The method as claimed in claim 1, further comprising forming transistors on the active area in the memory cell array region and in the supporting region.

13. A double corner rounding process for a partial vertical cell, comprising:

providing a substrate comprising a memory cell array region and a supporting region and having a first mask layer thereon, wherein a deep trench is formed in the first mask layer and the substrate in the memory cell region, a capacitor is formed in a lower portion of the deep trench, a first insulating is formed in the upper portion of the deep trench, the surface of the first insulating layer is lower than that of the substrate, and a shallow trench is formed to define active areas in the memory cell array region and the supporting region;

removing the edge of the first mask layer until the corner of the substrate is exposed;

performing a first rounding on the corner of the substrate;

conformally forming a second insulating layer on the first mask layer , the first insulating layer, and the substrate;

forming an insulating plug on the second insulating layer, such that the surface of the insulating plug is substantially level with that of the second insulating layer on the substrate;

removing the insulating plug, the second insulating layer, and the first mask layer from the memory

cell array to expose the corner of the substrate in the memory cell array region;

performing a second rounding process on the corner of the substrate in the memory cell array region.

14. The method as claimed in claim 13, wherein the first mask layer comprises stacked silicon oxide and silicon nitride layers.

15. The method as claimed in claim 13, wherein removal of the edge of the first mask layer is performed by anisotropic etching.

16. The method as claimed in claim 15, wherein an etching solution comprising hydrogen fluoride (HF) and ethylene glycol (EG) is employed in anisotropic etching.

17. The method as claimed in claim 13, wherein the first rounding process comprises oxidizing the corner and the sidewall of the first portion of the substrate to form a sacrificial oxide layer and removing the sacrificed oxide layer.

18. The method as claimed in claim 17, wherein oxidization is performed by in-situ steam generation (ISSG).

19. The method as claimed in claim 13, wherein the second insulating layer comprises silicon nitride.

20. The method as claimed in claim 1, wherein the insulating plug comprises silicon oxide formed by high density plasma chemical vapor deposition (HDP CVD).

21. The method as claimed in claim 13, wherein the second rounding process is performed by employing an oxidation agent and a HF solution by turns.

22. The method as claimed in claim 21, wherein the oxidation agent comprises $H_2O_{2(aq)}$ and $HNO_{3(aq)}$.

23. The method as claimed in claim 13, further comprising forming transistors on the active area in the memory cell array region and in the supporting region.